芯引领 · 源未来

高耐压低功耗原边反馈芯片

CY305X

器件手册

版本： A3

著作权

版本修订记录

版本号	更新日期	修订内容
A1	2019-10-08	初始版本
A2	2020-12-11	更改芯片封装
A3	2021-08-13	正式版本，修改公司地址，联系方式及封装说明

联系方式

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Features

▲Low Cost Solution Built-in 800V power BJT
▲Quasi-Resonant Primary Side Regulation (QR-PSR) Control with High Efficiency
▲Multi-Mode PSR Control
▲Fast Dynamic Response
▲Built-in Dynamic Base Drive
▲Audio Noise Free Operation
▲±5% CC and CV Regulation
▲Low Standby Power <70mW
▲Programmable Cable Drop Compensation (CDC) in CV Mode
▲Built-in AC Line & Load CC Compensation
▲Build in Protections:
- **Short Load Protection (SLP)**
- **Cycle-by-Cycle Current Limiting**
- **Leading Edge Blanking (LEB)**
- **Pin Floating Protection**
- **VDD OVP & UVP & Clamp**

▲Available with CY305X Versions in SOP-8 Package

Applications

■Battery Chargers for cellular phones, cordless phone, PDA, digital cameras, etc.
■Replaces linear transformer and RCC SMPS
■Small power adapter
■AC/DC LED lighting

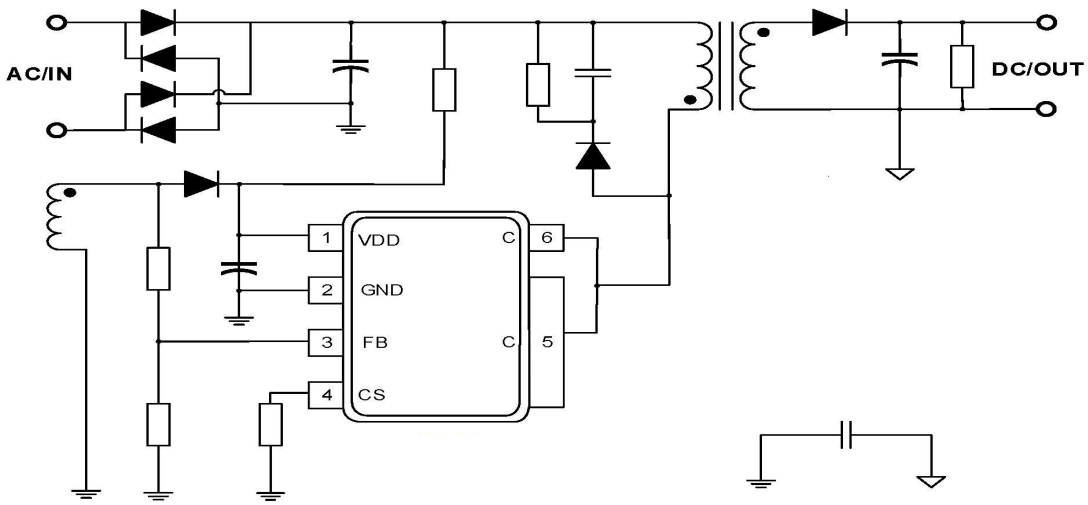
General Description

CY305X is a high performance Quasi Resonant (QR) Primary Side Regulation (PSR) PWM power switch with high precision CV/CC control ideal for charger applications.

In CV mode, CY305X adopts Multi Mode QR Control which uses the hybrid of AM (Amplitude Modulation) mode and (Frequency Modulation) FM mode to improve system efficiency and reliability. In CC mode, the IC uses PFM control with line and load CC compensation. The IC can achieve fast dynamic response. The built-in Cable Drop Compensation (CDC) function can provide excellent CV performance.

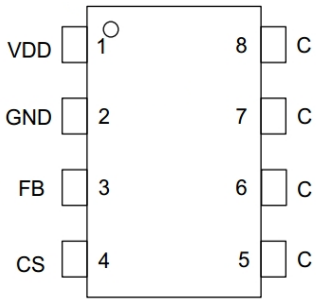
CY305X integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), VDD Clamping, etc.

Typical Application Information



General Information

Pin Configuration



CY305X

Absolute Maximum Ratings

Parameter	Value
HV PIN Maximum Voltage	800V
HV PIN DC Current	800mA
VDD DC Supply Voltage	30V
VDD DC Clamp Current	10mA
CS, BASE Voltage Range	-0.3 to 7V
FB Voltage Rage	-0.7 to 7V
R θ JA(℃/W) (SOP-7)	90℃/W
Maximum Junction Temperature	150℃
Operating Temperature Range	-40 to 85℃
Storage Temperature Range	-65 to 150℃
Lead Temperature (Soldering,10Sec.)	260℃
ESD Capability, HBM	±2KV
ESD Capability, MM	±400V

Recommended Operating Conditions

Parameter	Value	Unit
Supply Voltage, VDD	7 to 24	V
Operating ambient temperature	-40 to 80	℃
Maximum Switching Frequency@ Full Loading	70	KHz
Minimum Switching Frequency@ Full Loading	35	KHz

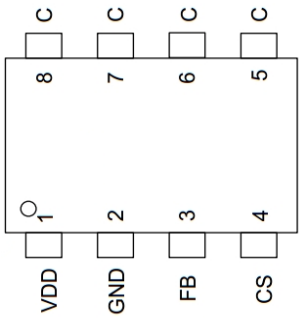
Output power meter

Chip model	100Vac ~265Vac
CY3056	12W
CY3058	14W
CY3059	16W

Pin Description

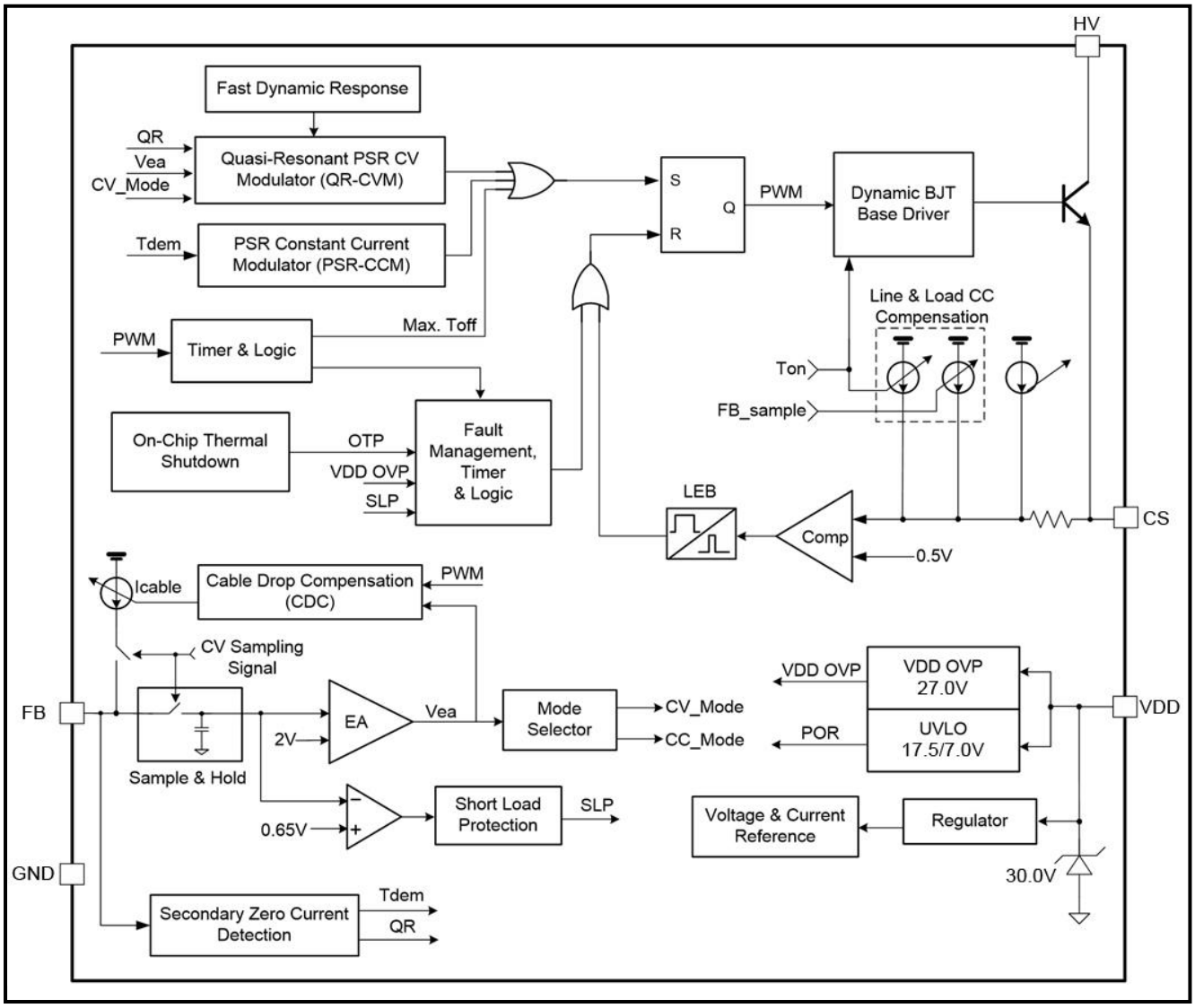
Pin No.	Name	I/O	Function
1	FB	I	System feedback pin which regulates both the output voltage in CV Mode and output current in CC mode based on the flyback voltage of The auxiliary winding
2	GND	P	The Ground of the IC
3	VDD	P	Power Supply Pin of the Chip
4	CS	I	Current Sense input Pin
5/6/7/8	C	O	The Power BJT Collector

Ordering and Marking Information



CYpoweric：Company Logo
CY305X：Product name
6F：Internal Code
15：Year Code
12：Week Code

BLOCK DIAGRAM

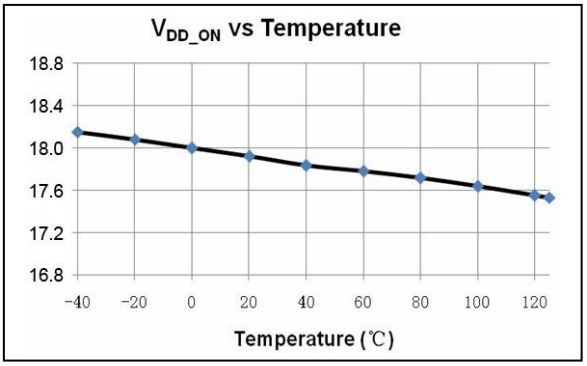


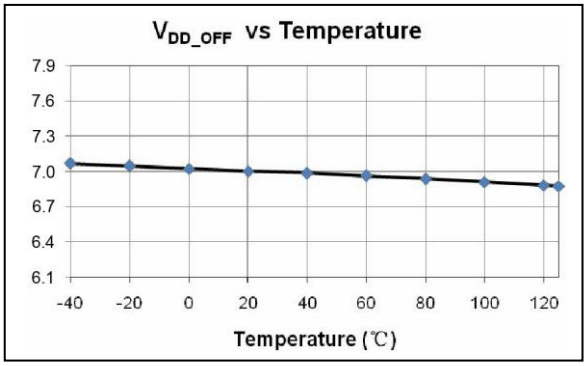
Electrical Characteristics

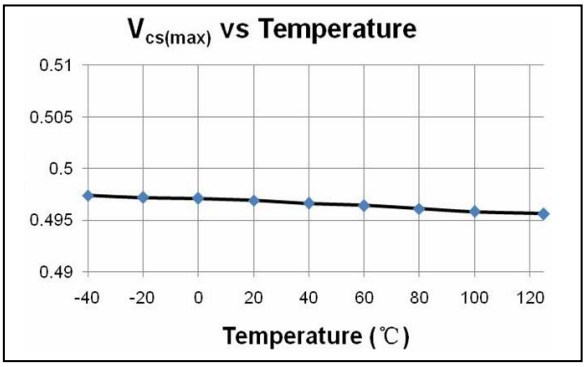
(T_A=25℃, unless otherwise stated, VCC=16.0V)

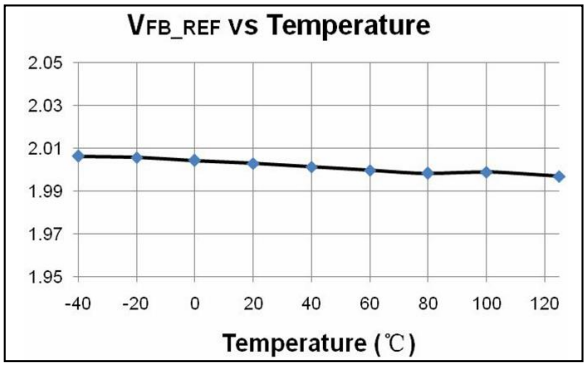
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE (VDD PIN)						
I_Startup	VDD Start up Current	VDD=16V, Measure current into VDD		3	5	uA
I_VDD_OP	Operation Current	VDD=20V		0.3	0.4	mA
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		15	16.5	18	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		5.5	6.0	6.5	V
V_{DD}_Clamp	VDD Over Voltage Protection trigger	I(V_{DD})=10mA	25	27	29	V
Feedback Input Section(FB Pin)						
V_{FB}_EA_Ref	Internal Error Amplifier(EA) reference input		1.97	2.00	2.03	V
V_{FB}_DEM	Demagnetization Comparator threshold			25		mV
T_{min}_OFF	Minimum OFF time			2		uS
T_{max}_OFF	Maximum OFF time			5		mS
T_{FB}_Short	Output Short Circuit Debounce Time			13		mS
T_{CC}/T_{DEM}	Ratio between switching period in CC mode and demagnetization time			2		
I_{Cable}_max	Max Cable compensation current			50		uA
Current Sense Input Section (CS Pin)						
T_blanking	CS Input Leading Edge Blanking Time			500		nS
Vth_OC	Current Limiting Threshold		480	500	520	mV
T_D_OC	Over Current Detection and Control Delay			100		nS
BJT Section (HV PIN)						
V_{CEO}	Collector-Emitter Voltage			480		V
V_{CBO}	Collector-Base Voltage			800		V

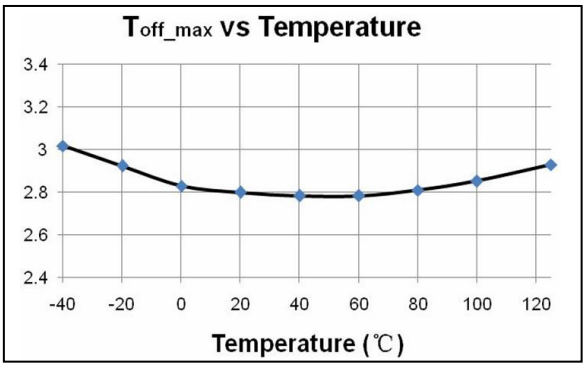
Characterization Plots

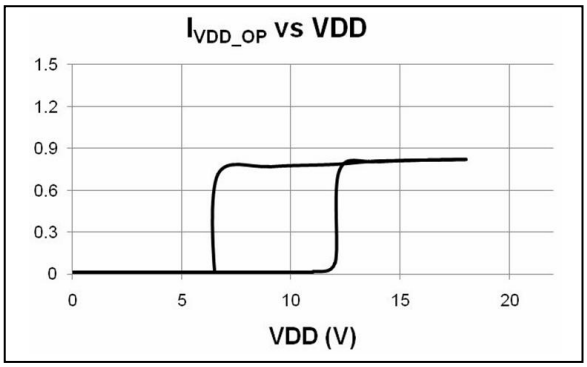












Operation Description

CY305X is a high performance, multi-mode, highly integrated Quasi Resonant Primary Side Regulation (QR-PSR) power switch. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications.

System Start-Up Operation

Before the IC starts to work, it consumes only startup current (typically 3uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches UVLO turn-on voltage of 17.5V (typical), CY305X begins switching and the IC operation current is increased to be 0.8mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage.

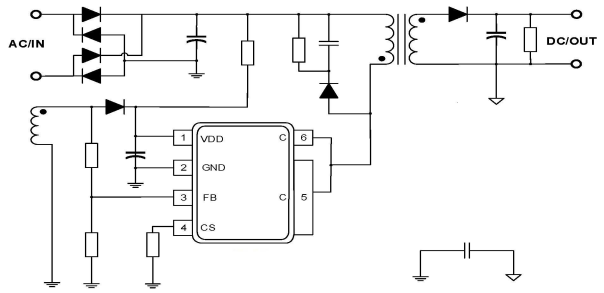


Fig.1

Once CY305X enters very low frequency FM (Frequency Modulation) mode, the operating current is reduced to be 500uA typically, which helps to reduce the standby power loss.

Quasi Resonant PSR CV Modulation (QR-CVM)

In Primary Side Regulation (PSR) control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. Fig.2 illustrates the timing waveform of CV sampling signal, demagnetization signal (DEM) and quasi-resonant (QR) trigger signal in CY305X. When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the Quasi Resonant PSR CV Modulator (QR-CVM) for CV regulation. A valley is selected to trigger new PWM cycle by the output of the QR-CVM bock, which is determined by the load. The internal reference voltage for EA is trimmed to 2V with high accuracy.

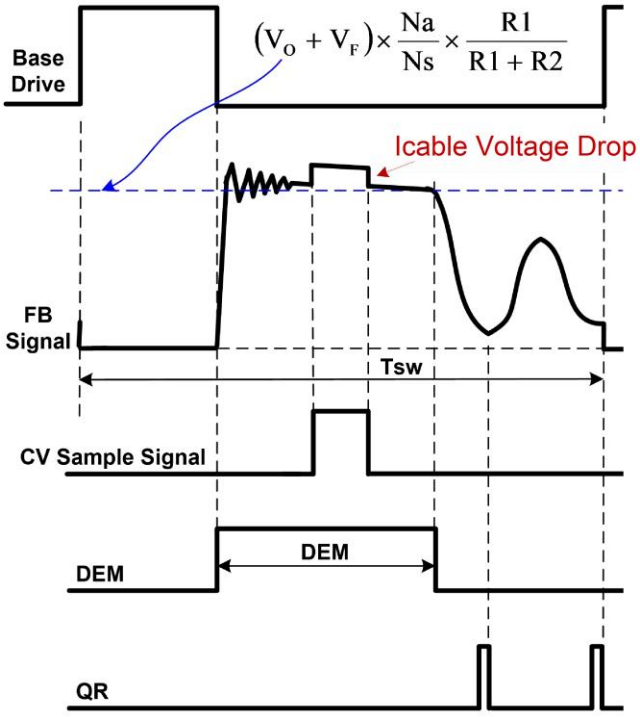


Fig.2

During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in Fig.2. Fig.2 also illustrates the equation for “demagnetization plateau”, where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na are secondary winding and auxiliary winding respectively.

When heavy load condition, the Mode Selector (as shown in “**Block Diagram**”) based on EA

output will switch to CC Mode automatically.

PSR Constant Current Modulation (PSR-CCM)

Timing information at the FB pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at I_{PP} (max), as shown in Fig.3.

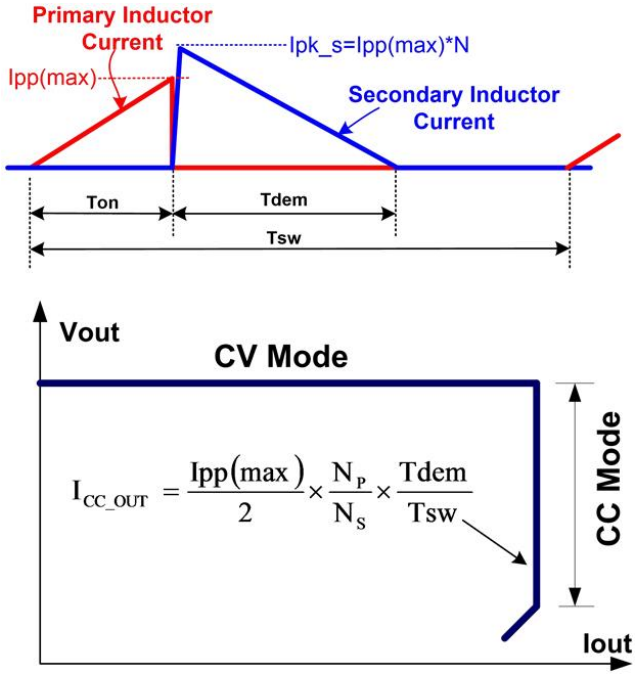


Fig.3

Referring to Fig.3 above, the primary peak current, transformer turns ratio, secondary demagnetization time (Tdem), and switching period (Tsw) determines the secondary average output current Iout. Ignoring leakage inductance effects, the equation for average output current is shown in Fig.3. When the average output current Iout reaches the regulation reference in the Primary Side Constant Current Modulator (PSR-CCM) block, the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

In CY305X, the ratio between Tdem and Tsw in CC mode is 1/2. Therefore, the average output current can be expressed as:

$$I_{CC\_OUT}(mA) \cong \frac{1}{2} \times N \times \frac{500mV}{Rcs(\Omega)}$$

In the equation above,

N- The turn ratio of primary side winding to secondary side winding.

Rcs-The sensing resistor connected between the power BJT emitter to GND.

Multi Mode Control in CV Mode

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in CY305X which is shown in the Fig 4.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 70mW.

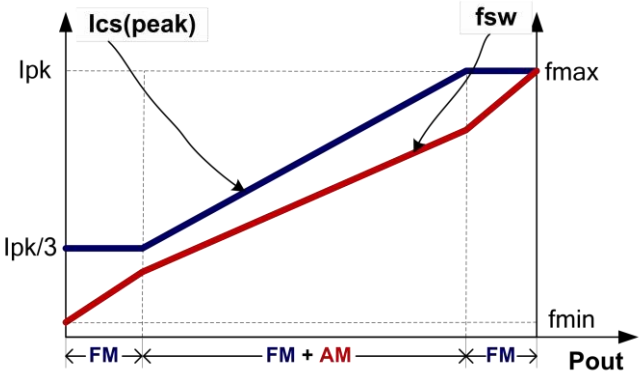


Fig.4

Programmable Cable Drop Compensation (CDC) in CV Mode

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In CY305X, an offset voltage is generated at FB pin by an internal

current

source (modulated by CDC block, as shown in Fig.5) flowing into the resistor divider. The current is proportional to the switching period, thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of R1 and R2 (as shown in Fig.), the cable loss compensation can be programmed. The percentage of maximum compensation is given by

$$\frac{\Delta V(cable)}{Vout} \cong \frac{Icable\_\max \times (R1 \parallel R2)}{V_{FB\_REF}} \times 100\%$$

For example, R1=3KΩ, R2=18KΩ, The percentage of maximum compensation is given by:

$$\frac{\Delta V(cable)}{Vout} \cong \frac{10uA \times (5K \parallel 30K)}{2V} \times 100\% \cong 2.5\%$$

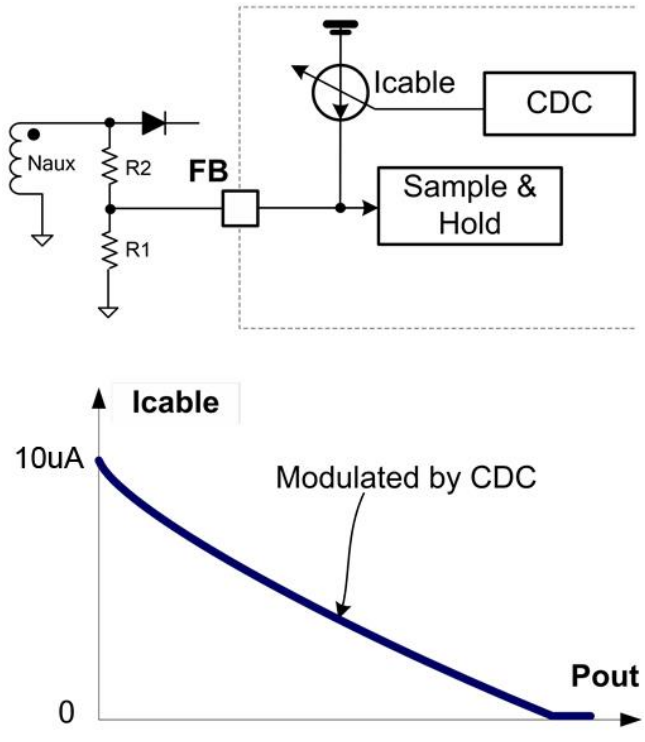


Fig.5

Optimized Dynamic Response

In CY305X, the dynamic response performance is optimized to meet USB charge requirements.

Audio Noise Free Operation

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation. An internal current source flowing to CS pin realizes CS peak voltage modulation. In CY305X, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

Dynamic BJT Base Drive

CY305X drive a power BJT with dynamic base drive control to optimize efficiency. The BJT base drive current ranges from 12mA to 35mA (typical), and is dynamically controlled according to the power supply load change. The higher the output power, the higher the based current. Specifically, the base current is related to CS peak voltage, as shown in Fig.6

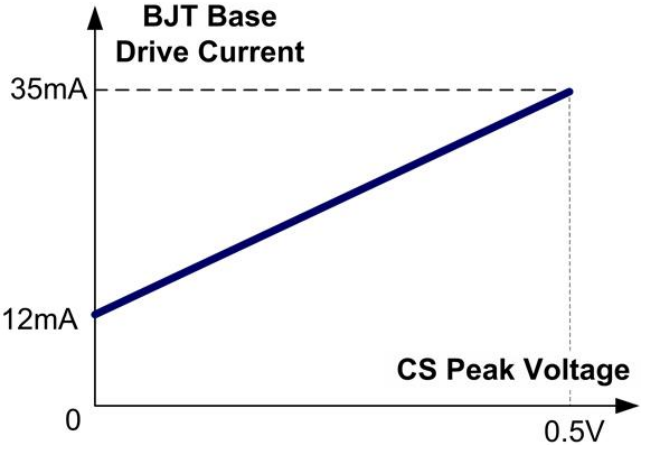


Fig.6

Short Load Protection (SLP)

In CY305X, the output is sampled on FB pin and then compared with a threshold of UVP (0.65V typically) after an internal blanking time (10ms typical).

In CY305X, when sensed FB voltage is below 0.6V, the IC will enter into Short Load Protection (SLP)

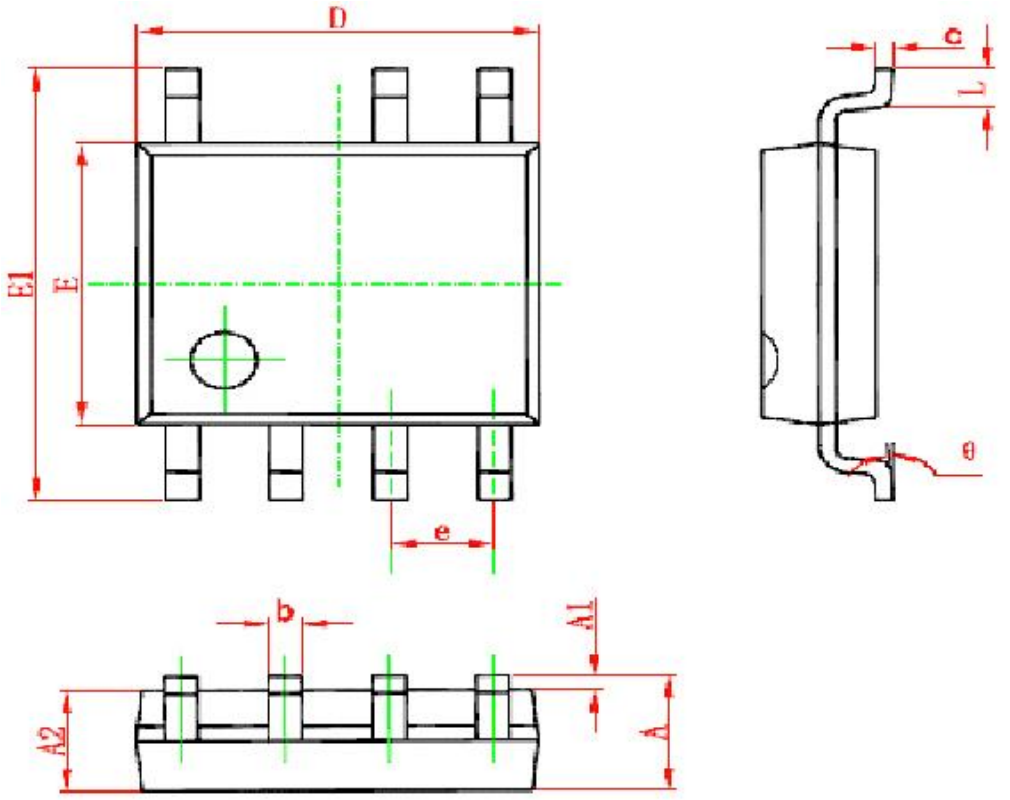
mode, in which the IC will enter into auto recovery protection mode.

VDD Over Voltage Protection (OVP) and Zener Clamp

When VDD voltage is higher than 27.0V (typical), the IC will stop switching. This will cause VDD fall down to be lower than VDD_OFF (typical 7.0V) and then the system will restart up again. An internal 30V (typical) zener clamp is integrated to prevent the IC from damage.

Package Information

SOP-7



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
B	0.310	0.510	0.012	0.020
C	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.05(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°